http://navajotech.edu
Tel: (505) 387-7401

Course Title: Intro. to VHDL and FPGA Course #: EE230

Credit Hours: 3hrs Semester: Spring 2022 Cap: 15

Faculty: Conrad Begay E-mail: conrad.begay@navajotech.edu

Office: N/A Office Phone: (505)906-5138

Office Hours: email

Preferred Communication email and/or text; will respond within 24 hours

Class Location: Hybrid / MOD16B

Class Meeting Times: 2:00pm to 3:15pm (Monday/Wednesday)

Required Materials: Desktop/laptop, Quartus II web edition,

Textbooks:

(Lecture) - VHDL for Engineers, 1st edition, Pearson, Kenneth L. Short, ISBN-13: 978-0-13-605843-4

(Reference) - Digital Electronics: A Practical Approach with VHDL, 9th edition, Pearson, Kleitz, William, ISBN-13:978-0-13-254303-3

Course Description

The goal of the course is to introduce digital design techniques using field programmable gate arrays (FPGAs). This course will cover FPGA architecture, digital design flow and other technologies associated with field programmable gate arrays. The course will involve an extensive amount of labs and projects which will give the students hands-on experience on designing digital systems on FPGA platforms.

Course Outcomes	Course Measurements
A strong understanding of fundamental digital IC	Complete Homework assignments, quizzes,
design.	exams, and projects
A strong understanding of fundamental digital IC	
design.	

A strong understanding of FPGA programming
techniques.
A strong understanding of FGPA sequential circuits
A strong understanding of timing issues
A strong understanding of VHDL

Connections to Program Assessment (course-embedded measures) List program outcomes to be measured

- 1. Fundamentals in digital IC design
- 2. FPGA & CPLD Architectures
- 3. FPGA Programming Technologies
- 4. FPGA Sequential Circuits
- 5. Timing Issues in FPGA Synchronous Circuits
- 6. Introduction to Verilog HDL and FPGA Design flow with using Verilog HDL

General Education Assessment List general education Outcomes to be measured

- 1. Ability to utilize the top-down design methodology in the design of highly complex digital devices such as FPGAs/ASICs.
- 2. Ability to use learn/use modern hardware/software design tools to develop modern digital systems
- 3. Ability to design verification and test of integrated circuits chips
- **4.** Ability to design, implement and test different Field Programmable Gate Array (FPGA) architectures and their Applications to real life such as cell phones, PDAs, etc.
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Course Activities

Week	Date	Chapters/Reading	Assignments	Assessments
1	Jan 24 - 28	Introduction to EE207		
	Jan 21	Last day to add/drop		
2	Jan 31 – Feb 4	Chapter 1		✓
3	Feb 7 - 11	Chapter 2, Lab1, & Quiz1	✓	✓
4	Feb 14 -18	Chapter 3, Lab2	✓	✓
5	Feb 22 - 25	Chapter 4, Lab3 & Quiz2	✓	✓
	Feb 25	Graduation Petition is due		
6	Feb 28 – Mar 4		Midterm	
7	Mar 7 - 11	Midterm grades are due		
8	Mar 14 - 18	Chapter 5 & Lab4	✓	✓
9	Mar 21 - 25	Chapter 6, Lab5 & Quiz3	✓	✓
	Mar 31	Last day to withdraw with a "W"		
10	Mar 28 - 31	Chapter 7 & Lab6	✓	✓

11	Apr 4 - 8	Lab7	✓	
12	Apr 11 - 15	Lab7 & Quiz4	✓	✓
13	Apr 18 - 22	Lab8	✓	
14	Apr 25 - 29	Final Project	✓	
15	May 2 - 6	Final Project	✓	
16	May 9 - 12		Finals	
	May 12	Grades are due to the Registrar		
	May 13	Spring Graduation		

Grading Plan

Homework	25%	A = 100 - 90%
Mid-Term	25%	B = 89 - 80%
Final Exam	25%	C = 79 - 70%
Quiz	10%	D = 69 - 60%
Final Project	10%	F<59%
Class Participation	3%	
Portfolio	2%	

Grading Policy

Each student must do his or her own homework and case studies. Discussion among students on homework and cases is encouraged for clarification of assignments, technical details of using software, and structuring major steps of solutions - especially on the course's Web site. Students must do their own work on the homework and exam. Cheating and Plagiarism are strictly forbidden. Cheating includes but is not limited to: plagiarism, submission of work that is not the student's own, submission or use of falsified data, unauthorized access to exam or assignment, use of unauthorized material during an exam, supplying or communicating unauthorized information for an assignment or exam.

Participation

Students are expected to attend and participate in all class activities- as listed above, as it is 3% of the grade. Points will be given to students who actively participate in class activities including field trips, laboratories, and ask questions of guest speakers and other presenters.

Cell phone and headphone use

Please turn cell phones off or place them on silence or vibrate mode **before** coming to class. Also, answer cell phones **outside of class** (not in the classroom). Exercising cell phone use courtesy is appreciated by both the instructor and classmates. Headphones are to be removed before coming to class.

Attendance Policy

Students are expected to regularly attend all classes for which they are registered. A percentage of the student's grade will be based on class attendance and participation. Absence from class, regardless of the reason, does not relieve the student of his/her responsibility to complete all course work by the required deadlines. Furthermore, it is the student's responsibility to obtain notes, handouts, and any other information covered when absent from class and to arrange to make up any in-class assignments or tests if permitted by the instructor. Incomplete or missing assignments will necessarily affect the student's grades. Instructors will report excessive and/or unexplained absences to the Counseling Department for investigation and potential intervention. Instructors may drop students from the class after three (3) absences unless prior arrangements are made with the instructor to make up work and the instructor deems any excuse acceptable.

Study Time Outside of Class for Face-to-Face Courses

For every credit hour spent in a class, a student is expected to spend two hours (2) outside of class studying the course materials.

Study Time for Hybrid or Blended Courses

For a hybrid or blended course of one (1) credit hour, a student is expected to spend three (3) hours per week studying the course materials.

Study Time for Online Courses

For an online course of one (1) credit hour, a student is expected to spend four hours (4) per week studying the course materials.

Academic Integrity

Integrity (honesty) is expected of every student in all academic work. The guiding principle of academic integrity is that a student's submitted work must be the student's own. Students who engage in academic dishonesty diminish their education and bring discredit to the University community. Avoid situations likely to compromise academic integrity such as: cheating, facilitating academic dishonesty, and plagiarism; modifying academic work to obtain additional credit in the same class unless approved in advance by the instructor, failure to observe rules of academic integrity established by the instructor. The use of another person's ideas or work claimed as your own without acknowledging the original source is known as plagiarism and is prohibited.

Diné Philosophy of Education

The Diné Philosophy of Education (DPE) is incorporated into every class for students to become aware of and to understand the significance of the four Diné philosophical elements, including its affiliation with the four directions, four sacred mountains, the four set of thought processes and so forth: Nitsáhákees, Nahát'á, Íína and Siih Hasin which are essential and relevant to self-identity, respect and wisdom to achieve career goals successfully.

Students with Disabilities

The Navajo Technical University and the Electrical Engineering Department are committed to serving all enrolled students in a non-discriminatory and accommodating manner. Any student who feels he/she may need an accommodation based on the impact of disability or needs special accommodations should inform NTU in accordance with the procedures of the subsection entitled "Students with Disabilities" under Section 7: Student Support Programs, NTU Student Handbook.

Email Address

Students are required to use NTU's email address as a formal mode of communication.

Final Exam Date:

05/09/2022